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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	JOYCE S. OEY HEWETT ALEXANDER J. PASADYN	§	**Group Art Unit:**	2823
Serial No.:	09/909,074	§		
Filed:	July 19, 2001	§	**Examiner:**	Khiem D. Nguyen
Title:	Method and Apparatus for Controlling a Thickness of a Conductive Layer in a Semiconductor Manufacturing Operation	§	**Docket No.**	2000.075200/TT4629

Mail Stop Appeal Brief – Patents
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P.O. Box 1450
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9-2-03 Vicki Baudino
Date Signature

APPEAL BRIEF

Dear Sir:

Applicant hereby submits an original and two copies of this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final rejection mailed on March 12, 2003.

Assistant Commissioner is authorized to deduct a fee in the amount of $320.00 and any additional fees required under 37 C.F.R. §§ 1.16 to 1.21 from the Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT4629. In the event the monies in that account are insufficient, the Assistant Commissioner is authorized to withdraw funds from the Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.075200/DCD.

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc. The assignment of the present application is recorded at Reel 012012, Frame 0191.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1, 2, 4-13, and 15 have been finally rejected and are the subject of this appeal. More specifically:

- claims 1, 2, 4, and 5 stand rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent Application Publication No. 2002/0032499 to Wilson *et al.* (hereinafter referred to as "the Wilson application") in view of U.S. Patent No. 4,405,677 to Chen (hereinafter referred to as "the Chen patent"); and
- claims 6-13 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being obvious over the Wilson application in view of the Chen patent.

While all pending claims are rejected under 35 U.S.C. §103(a) over the Wilson application in view of the Chen patent, separate rejections were made in the Final Office Action of March 12, 2003. The rejections are separately addressed herein, since "[f]or each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection and, if appropriate, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and shall explain how such limitations render the claimed subject matter unobvious over the prior art." *See* 37 C.F.R. §1.192(c)(8)(iv).

IV. STATUS OF AMENDMENTS

There were no amendments to the claims after the final Office Action. The claims as currently pending on appeal are attached as Appendix A.

V. SUMMARY OF THE INVENTION

Generally, the present invention relates to a method of controlling a thickness of a deposited, conductive layer in integrated circuit devices. When considering forming conductive interconnects comprised of copper, the process of forming conductive layers, such as leads, interconnects, contacts, vias, plugs, and the like, generally involves, among other things, deposition of a conductive seed layer followed by formation of a bulk conductive layer using known electroplating techniques. Such bulk conductive layers typically undergo a chemical mechanical planarization step, wherein the exposed surface of the conductive layer is planarized and the thickness of the conductive layer is brought into tolerance. The thickness of the as-deposited bulk conductive layer is important for a number of reasons. For example, if the thickness of the as-deposited bulk conductive layer is below the tolerance range, there may be insufficient material within the conductive layer to conduct electrons. If the thickness of the as-deposited bulk conductive layer is too large, additional time may be required in the chemical mechanical planarization step to remove the excess material. In conventional semiconductor wafer manufacturing, the thickness of these bulk conductive layers typically are not monitored or they are only checked on a lot-by-lot basis. Therefore, even if the thicknesses of the conductive layers are checked on a lot-by-lot basis, adjustments to the deposition process can generally be made no more frequently than between lots. *See* Patent Application, page 2, lines 1-14. Thus, it is desirable to measure and control the thickness of bulk conductive layers on a wafer-by-wafer basis.

Accordingly, Applicants describe, and claim in independent claim 1:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer deposited on the semiconductor wafer;

determining whether the measured thickness of the conductive layer is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance.

Applicants also describe, and claim in independent claim 6:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer at a plurality of locations;

calculating a value representing the measured thickness measured at the plurality of locations;

determining whether the calculated value is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least the calculated value if the calculated value is not within the predetermined tolerance.

For example, if the thickness of the conductive layer 206 on semiconductor wafer *J* is not within tolerance or if the calculated value representing the plurality of thickness measurements in the aggregate is not within tolerance, a control unit 610 takes one or more actions so that the conductive layer on the next wafer (*i.e.*, wafer *J*+1) will have a thickness within tolerance (block 308). Such actions may include revising a chemical concentration of the electroplating bath in which the conductive layer 206 of the wafer *J*+1 is to be deposited and/or changing the anode-cathode spacing for the deposition of the conductive layer 206 on the wafer *J*+1. *See* Patent Application, page 9, ll. 11-18 and FIGS. 2 and 3.

Alternatively, if the thickness of the conductive layer 206 on the wafer *J* is within tolerance, the next wafer (*i.e.*, wafer *J*+1) is processed (blocks 310, 302) with no changes to the deposition recipe. *See* Patent Application, page 9, ll. 20-22.

VI. ISSUES ON APPEAL

Appellant respectfully requests that the Board review and overturn the two rejections present in this case:

A. Are claims 1, 2, 4, and 5 obvious over the Wilson application in view of the Chen patent?

B. Are claims 6-13 and 15 obvious over the Wilson application in view of the Chen patent?

As shown more fully below, it is respectfully submitted that the Examiner erred in rejecting the pending claims.

VII. GROUPING OF THE CLAIMS

For the issues presented above, claims 1, 2, 4-13, and 15 can be considered to stand or fall together.

VIII. ARGUMENT

A. Claims 1, 2, 4, and 5 are not obvious over the Wilson application in view of the Chen patent.

As the Board well knows, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the

combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142.

Claims 1, 2, 4, and 5 should be allowed over the cited references, because:

- the cited references, either singly or in combination, fail to disclose all of the limitations of the rejected claims;
- the Chen patent teaches away from the claimed invention; and
- the Chen patent is a nonanalogous reference.

The cited references fail to disclose all of the limitations of the rejected claims.

The Wilson application is generally directed to an apparatus for automatically selecting and refining electrical parameters for processing microelectronic workpieces. However, the Examiner admits that the Wilson application fails to disclose revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance, as required by claim 1. *See* page 3, lines 5-8, of the Final Office Action. The Examiner relies on the Chen patent for a teaching that the thickness of the conductive layer may be controlled by varying

the chemical concentration of the electroplating bath. *See* page 3, lines 9-11, of the Final Office Action. However, as shown in FIG. 6 below and described thereafter, the Chen patent fails to disclose or suggest the limitations of claim 1:

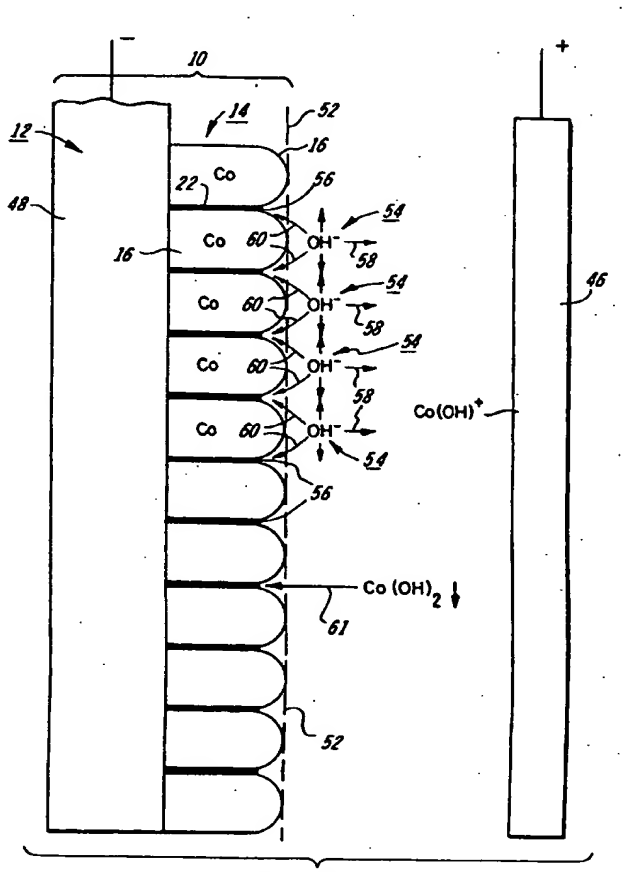

FIG. 6

The Chen patent discloses that a plated film 14 comprises a plurality of particles 16 disposed on a substrate 12. *See* column 5, lines 1-2, of the Chen patent. The Examiner incorrectly alleges that the Chen patent (in column 8, lines 5-17) teaches that the thickness of the film 14 may be controlled by varying the chemical concentration of the plating solution. In fact, the Chen patent teaches, in column 8, lines 5-17, that the thickness of the film 14 is determined by the length of time of electroplating and that the width of the particles 16 may be controlled by varying conditions such as the concentration of cobalt ions:

> *Generally, the width of the particles 16 and the extent of separation between the particles, i.e., the width of the intergranual boundary 22 in the*

plated film 14, may be controlled by varying the electroplating bath conditions, such as, by the concentration of Co^{++} ions in the plating solution, pH value of the solution, the temperature of the electroplating bath or by the deposition rate of the particles as defined by the current density of the electroplating process. The length of the acicular particles 16 or the ***thickness*** *of the film 14 is principally determined by the length of time of electroplating. The length to width ratio of the particles may be, for example, 3:1.* [Emphasis added]

Applicants respectfully submit that if one skilled in the art at the time of the invention were to combine the Wilson application and the Chen patent, the result would be an apparatus that changes the length of electroplating time to correct errors in thickness of a deposited layer.

Thus, by admission of the Office, the Wilson patent fails to disclose or suggest revising either the chemical concentration of the electroplating bath or the anode-cathode spacing of the deposition recipe, as required by claim 1. Further, the Chen patent, contrary to the Examiner's allegation, fails to disclose or suggest changing either the chemical concentration or the anode-cathode spacing. Thus, the cited references fail to disclose all of the limitations of the rejected claims. Claims 1, 2, 4, and 5, therefore, should be allowed, as the Office has failed to establish a *prima facie* case of obviousness. "When the references cited by the examiner fail to establish a *prima facie* case of obviousness, the rejection is improper and will be overturned. *In re Brouwer*, 37 U.S.P.Q.2d (BNA) 1663, 1666 (Fed. Cir. 1995); *In re Ochiai*, 37 U.S.P.Q.2d (BNA) 1127, 1131 (Fed. Cir. 1995).

The Chen patent teaches away from the claimed invention.

The Chen patent distinguishes between controlling the width of the particles 16 and controlling the thickness of the film 14. The Chen patent teaches that the width of the particles 16 may be controlled by controlling various parameters, such as by controlling the concentration of cobalt ions in the electroplating bath. Furthermore, the Chen patent points out that the thickness of the film 14 is controlled by the length of electroplating time. If

varying the concentration of cobalt ions in the electroplating bath were applicable to controlling the thickness of the film 14, the Chen patent would not have made this distinction. However, by making this distinction, Applicants respectfully submit that the Chen patent teaches away from controlling the thickness of the film 14 by any other method, such as by revising the chemical concentration of the electroplating bath and the anode-cathode spacing of the deposition recipe. The Wilson application and the Chen application, therefore, cannot be properly combined to render the present invention, as set forth in claims 1, 2, 4, and 5, obvious. There can be no motivation or suggestion to combine references as a matter of law where one of the references teaches away from the claimed invention. *In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Gordon*, 221 U.S.P.Q. (BNA) 1125, 1127 (Fed. Cir. 1984).

The Chen patent is a nonanalogous reference.

As the Board is aware, "[t]wo criteria have evolved for determining whether prior art is analogous: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved." *In re Clay*, 966 F.2d 656, 658-59 (Fed. Cir. 1992) (reversing Board holding of obviousness).

The Chen patent is not in the same field of endeavor as the claimed subject matter merely because it relates to depositing a film or layer on a substrate. The present invention involves an integrated circuit device, in which layers are formed to conduct electrical signals. In contrast, the Chen patent relates to a magnetic recording medium, in which a film is formed to store or retain a magnetic charge. Furthermore, the different fields of endeavor are evidenced by different classifications in the Patent Office. The present invention is classified

in class 438, "Semiconductor Device Manufacturing: Process", described as providing "for manufacturing a semiconductor containing a solid-state device by a combination of operations", while the Chen patent is classified in class 428, "Stock Material or Miscellaneous Articles", described as being "directed to stock material composites, that is, materials having two or more distinct components which are more ordered than a mere random mixture of ingredients." For at least these reasons, Applicants respectfully assert that the Chen patent is not within the field of endeavor of the present invention.

As the Chen patent has been shown to be outside the field of endeavor of the present invention, it must be determined whether the Chen patent is reasonably pertinent to the particular problem with which Applicants were involved. The present invention concerns controlling the thickness of an electrically conductive layer formed on a semiconductor substrate. In contrast, the Chen patent concerns controlling the width and length of a multitude of acicular particles, physically separated by impurities or voids, that comprise a magnetic recording layer disposed on a conductive substrate. *See* column 4, line 64, through column 5, line 12, of the Chen patent. Since the Chen patent is directed to a different purpose than the claimed invention, one of ordinary skill in the art "would accordingly have had less motivation or occasion to consider it". *Clay*, 23 U.S.P.Q.2d (BNA) 1061. Applicants respectfully submit that if one skilled in the art of the present invention were to become aware of the Chen patent at the time of the present invention, the Chen patent would not have been considered, because it would have been appreciated that a process to produce a film having impurities or voids therein would not be desirable in the manufacture of integrated circuit devices, as the impurities or voids would hinder the conduction of electrical signals. Thus, the Chen patent is not pertinent to the particular problem addressed by the present invention and, as discussed above, is not within the field of Applicants' endeavor.

Thus, Applicants respectfully submit that claims 1, 2, 4, and 5 are not obvious over the Wilson application in view of the Chen patent and should be allowed, because the cited references fail to teach or suggest all of the claim limitations, the Chen patent teaches away from the claimed invention, and the Chen patent is a nonanalogous reference.

B. Claims 6-13 and 15 are not obvious over the Wilson application in view of the Chen patent.

Claims 6-13 and 15 should be allowed over the cited references, because:

- the cited references, either singly or in combination, fail to disclose all of the limitations of the rejected claims;
- the Chen patent teaches away from the claimed invention; and
- the Chen patent is a nonanalogous reference.

The cited references fail to disclose all of the limitations of the rejected claims.

Claims 6-13 are not obvious for the reasons set forth above with respect to claims 1, 2, 4, and 5. For the convenience of the Board and to ensure compliance with 37 C.F.R. §1.192(c)(8)(iv), those arguments are repeated again with respect to claims 6-13 and 15.

As discussed above, the Examiner admits that the Wilson application fails to disclose revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance, as required by claim 1. *See* page 4, line 21, through page 5, line 2, of the Final Office Action. The Examiner again relies on the Chen patent for a teaching that the thickness of the conductive layer may be controlled by varying the chemical concentration of the electroplating bath. *See* page 5, lines 3-6, of the Final Office Action. However, as shown in

FIG. 6 above, The Chen patent discloses that a plated film 14 comprises a plurality of particles 16 disposed on a substrate 12. *See* column 5, lines 1-2, of the Chen patent. The Examiner incorrectly alleges that the Chen patent (in column 8, lines 5-17) teaches that the thickness of the film 14 may be controlled by varying the chemical concentration of the plating solution. In fact, the Chen patent teaches, in column 8, lines 5-17, that the thickness of the film 14 is determined by the length of time of electroplating and that the width of the particles 16 may be controlled by varying conditions such as the concentration of cobalt ions:

> *Generally, the **width** of the particles 16 and the extent of separation between the particles, i.e., the width of the intergranual boundary 22 in the plated film 14, may be controlled by varying the electroplating bath conditions, such as, by the concentration of Co^{++} ions in the plating solution, pH value of the solution, the temperature of the electroplating bath or by the deposition rate of the particles as defined by the current density of the electroplating process. The length of the acicular particles 16 or the **thickness** of the film 14 is principally determined by the length of time of electroplating. The length to width ratio of the particles may be, for example, 3:1.* [Emphasis added]

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Thus, by admission of the Office, the Wilson patent fails to disclose or suggest revising either the chemical concentration of the electroplating bath or the anode-cathode spacing of the deposition recipe, as required by claim 1. Further, the Chen patent, contrary to the Examiner's allegation, fails to disclose or suggest changing either the chemical concentration or the anode-cathode spacing. Thus, the cited references fail to disclose all of the limitations of the rejected claims. Claims 1, 2, 4, and 5, therefore, should be allowed, as the Office has failed to establish a *prima facie* case of obviousness. "When the references cited by the examiner fail to establish a *prima facie* case of obviousness, the rejection is

improper and will be overturned. *In re Brouwer*, 37 U.S.P.Q.2d (BNA) 1663, 1666 (Fed. Cir. 1995); *In re Ochiai*, 37 U.S.P.Q.2d (BNA) 1127, 1131 (Fed. Cir. 1995).

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reference still is reasonably pertinent to the particular problem with which the inventor is involved." *In re Clay*, 966 F.2d 656, 658-59 (Fed. Cir. 1992) (reversing Board holding of obviousness).

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As the Chen patent has been shown to be outside the field of endeavor of the present invention, it must be determined whether the Chen patent is reasonably pertinent to the particular problem with which Applicants were involved. The present invention concerns controlling the thickness of an electrically conductive layer formed on a semiconductor substrate. In contrast, the Chen patent concerns controlling the width and length of a multitude of acicular particles, physically separated by impurities or voids, that comprise a magnetic recording layer disposed on a conductive substrate. *See* column 4, line 64, through column 5, line 12, of the Chen patent. Since the Chen patent is directed to a different purpose than the claimed invention, one of ordinary skill in the art "would accordingly have had less

motivation or occasion to consider it". *Clay*, 23 U.S.P.Q.2d (BNA) 1061. Applicants respectfully submit that if one skilled in the art of the present invention were to become aware of the Chen patent at the time of the present invention, the Chen patent would not have been considered, because it would have been appreciated that a process to produce a film having impurities or voids therein would not be desirable in the manufacture of integrated circuit devices, as the impurities or voids would hinder the conduction of electrical signals. Thus, the Chen patent is not pertinent to the particular problem addressed by the present invention and, as discussed above, is not within the field of Applicants' endeavor.

Thus, Applicants respectfully submit that claims 6-13 and 15 are not obvious over the Wilson application in view of the Chen patent and should be allowed, because the cited references fail to teach or suggest all of the claim limitations, the Chen patent teaches away from the claimed invention, and the Chen patent is a nonanalogous reference.

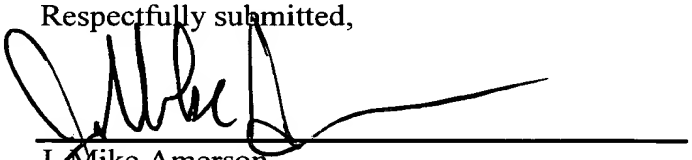
CONCLUSION

In view of the foregoing arguments, Applicants respectfully request that the Board of Patent Appeals and Interferences reverse the decision rejecting claims 1, 2, 4-13, and 15 and direct the Examiner to pass the case to issue.

WILLIAMS, MORGAN & AMERSON
CUSTOMER NUMBER: 23720

Date: September 2, 2003

Respectfully submitted,



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APPENDIX A

The claims on appeal are:

1. A method of controlling a conductive layer deposition process, comprising:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer deposited on the semiconductor wafer;

determining whether the measured thickness of the conductive layer is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance.

2. A method, according to claim 1, wherein:

depositing the conductive layer above the first semiconductor wafer further comprises depositing a copper layer above the first semiconductor wafer;

measuring the thickness of the conductive layer further comprises measuring the thickness of the copper layer;

determining whether the measured thickness of the conductive layer is within the predetermined tolerance further comprises determining whether the measured thickness of the copper layer is within the predetermined tolerance; and

revising the deposition recipe further comprises revising the deposition recipe if the measured thickness of the copper layer is not within the predetermined tolerance.

4. A method, according to claim 1, further comprising depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe.

5. A method, according to claim 1, wherein revising the deposition recipe further comprises revising the deposition recipe according to at least one predetermined model.

6. A method of controlling a conductive layer deposition process, comprising:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer at a plurality of locations;

calculating a value representing the measured thickness measured at the plurality of locations;

determining whether the calculated value is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least the calculated value if the calculated value is not within the predetermined tolerance.

7. A method, according to claim 6, wherein:

depositing the conductive layer above the first semiconductor wafer further comprises depositing a copper layer above the first semiconductor wafer; and

measuring the thickness of the conductive layer further comprises measuring the thickness of the copper layer at the plurality of locations.

8. A method, according to claim 6, wherein measuring the thickness of the conductive layer further comprises measuring the thickness of the conductive layer in a predetermined pattern of locations.

9. A method, according to claim 6, wherein calculating the value further comprises calculating an average of the plurality of thickness measurements.

10. A method, according to claim 6, wherein calculating the value further comprises calculating the value selected from the group consisting of an arithmetic mean of the plurality of thickness measurements, a median of the plurality of thickness measurements, a mode of the plurality of thickness measurements, a geometric mean of the plurality of thickness measurements, a harmonic mean of the plurality of thickness measurements, and a quadratic mean of the plurality of thickness measurements.

11. A method according to claim 6, wherein determining whether the thickness of the conductive layer is within the predetermined tolerance further comprises calculating a measure of a degree of dispersion of the plurality of thickness measurements about the calculated value and comparing the measure of the degree of dispersion to a predetermined statistical distribution.

12. A method, according to claim 6, wherein determining whether the thickness of the conductive layer is within the predetermined tolerance further comprises calculating a measure of a degree of dispersion of the plurality of thickness measurements about the calculated value representing the measured thicknesses and comparing the measure of the degree of dispersion to a distribution selected from the group consisting of a normal distribution, a binomial distribution, a Poisson distribution, and a multinomial distribution.

13. A method, according to claim 6, wherein revising the deposition recipe further comprises revising the deposition recipe according to at least one predetermined model.

15. A method, according to claim 6, further comprising depositing a conductive layer above a second semiconductor wafer based upon the revised deposition recipe.